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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,367	08/28/2001	Naoto Kusumoto	07977-010005	9947

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EXAMINER	
DOAN, THERESA T	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,367	KUSUMOTO ET AL.	
	Examiner	Art Unit	
	Theresa T Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *3-8,11-16 and 21-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,9,10 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *23 June 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/604,547* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 9-10 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (APA) in view of Asano (5,409,867) and Miyao et al. (U.S. Pat. 4,599,133) as previously cited.

APA teaches in the text pages 1-2 and figures 3A-3D a method of manufacturing a semiconductor device having at least one thin film transistor, the method comprising the steps of:

forming an amorphous silicon semiconductor layer 31 over a substrate;

irradiating the amorphous silicon semiconductor layer with a laser to crystallize the amorphous semiconductor layer; and

forming source, drain and channel region of the thin film transistor within the amorphous silicon semiconductor layer.

APA does not teach a linear laser beam is a second harmonic component having a wavelength of 532 nm generated from a continuous oscillating light source wherein the amorphous semiconductor layer is scanned with the linear laser beam in parallel with a carrier flow direction in the active regions (source, drain and channel regions).

Asano teaches in figures 1a-1e and columns 1-4 that a linear laser beam 4 is a second harmonic component having a wavelength of 532 nm generated from an pulse oscillating light source, wherein the amorphous semiconductor layer is scanned with the linear laser beam in parallel with a carrier flow direction in a semiconductor substrate (column 2, lines 59-68; column 3, lines 63-68 and column 4, lines 1-22) in order to reduce the accumulated distortion of the amorphous semiconductor layer and producing a polycrystalline semiconductor thin film which has a large grain size and can be used as a material for an active region of a semiconductor element (column 1, lines 50-53). Given the above teaching, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to apply the method of Asano in APA for reducing the accumulated distortion of the amorphous semiconductor layer and producing a polycrystalline semiconductor thin film which has a large grain size and can be used as a material for an active region of a semiconductor element.

It also would have been obvious to substitute the pulse oscillating light source for a continuous wavelength laser because as taught by Miyao, the continuous wavelength laser would provide better results than the pulse laser (column 5, lines 20-25).

3. Claims 1-2, 9-10 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (APA) in view of Asano (5,409,867) and Morita et al. (U.S. Pat. 4,468,853) as previously cited.

APA teaches in the text pages 1-2 and figures 3A-3D a method of manufacturing a semiconductor device having at least one thin film transistor, the method comprising the steps of:

forming an amorphous silicon semiconductor layer 31 over a substrate;

irradiating the amorphous silicon semiconductor layer with a laser to crystallize the amorphous semiconductor layer; and

forming source, drain and channel region of the thin film transistor within the amorphous silicon semiconductor layer.

APA does not teach a linear laser beam is a second harmonic component having a wavelength of 532 nm generated from a continuous oscillating light source wherein the amorphous semiconductor layer is scanned with the linear laser beam in parallel with a carrier flow direction in the active regions (source, drain and channel regions).

Asano teaches in figures 1a-1e and columns 1-4 that a linear laser beam 4 is a second harmonic component generated from a continuous oscillating light source, wherein the amorphous semiconductor layer is scanned with the linear laser beam in parallel with a carrier flow direction in a semiconductor substrate (column 2, lines 59-68; column 3, lines 63-68 and column 4, lines 1-22) in order to reduce the accumulated distortion of the amorphous semiconductor layer and producing a polycrystalline semiconductor thin film which has a large grain size and can be used as a material for an active region of a semiconductor element (column 1, lines 50-53). Given the above teaching, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to apply the method of Asano in APA for reducing the

accumulated distortion of the amorphous semiconductor layer and producing a polycrystalline semiconductor thin film which has a large grain size and can be used as a material for an active region of a semiconductor element.

APA and Asano do not disclose a continuous oscillating light source. However, Morita et al. disclose a second harmonic component having a wavelength of approximate 532 nm and generated from a continuous oscillating light source with a scanning speed of 60mm/sec (column 3, lines 54-62) in order to crystalline the semiconductor layer. Therefore, it would have been obvious to use either continuous oscillating laser or pulse oscillating laser with the second harmonic component having wavelength of approximate 532 nm as taught by Morita, because they both provide the same result of crystalline the semiconductor layer.

Response to Arguments

Applicant argues that "Asano is unclear as to how there moving directions are related to a carrier flow direction in the channel region". According to Applicant, "Asano does not disclose any process for forming the source and drain regions, and thus, does not describe any relationship between the irradiating direction and the carrier flow direction".

This argument is not persuasive because Asano clearly discloses that the semiconductor layer can be used as an **active region** of a semiconductor element (i.e., transistor) (column 4, lines 20-22). Therefore, the horizontal direction is a direction of a carrier flow, which is be parallel to the direction 3 of the light beam 4. Thus, Asano

clearly suggests the semiconductor layer being scanned with the laser beam in parallel with a carrier flow direction.

Also, Applicant argues that "with respect to claim 9, the references (APA, Asano and Miyao) fail to describe or suggest irradiating the semiconductor layer with the laser beam to crystallize a semiconductor layer while moving the substrate in a direction approximately perpendicular to a lengthy direction of the linear laser beam".

This argument is not persuasive because Asano in figure 1b discloses a linear laser beam 4 is moved in the direction of arrow 3 which approximately perpendicular to a lengthy direction of the linear laser beam. Evidently, Asano specifically states at column 2, lines 60-61 and column 4, lines 2-4:

"***As shown in Fig. 1(b), while the substrate 1 was moved in the direction of arrow 3 and in the direction normal thereto, it was irradiated with a light beam 4...***" and "***In this case, according to the continuous ray , ... the amorphous silicon layer is linearly crystallized.***"

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Thursday from 8:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TD
March 2, 2004.

PHAT X. CAO
PRIMARY EXAMINER